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QUERY CONTROL FORM		RTIS USE ONLY	
Application No.	Prepared by	Tracking Number	
Examiner-GAU	Date	Week Date	
	No. of queries		

JACKET

a. Serial No.	f. Foreign Priority	k. Print Claim(s)	p. PTO-1449
b. Applicant(s)	g. Disclaimer	l. Print Fig.	q. PTOL-85b
c. Continuing Data	h. Microfiche Appendix	m. Searched Column	r. Abstract
d. PCT	i. Title	n. PTO-270/328	s. Sheets/Figs
e. Domestic Priority	j. Claims Allowed	o. PTO-892	t. Other

SPECIFICATION

- a. Page Missing
- b. Text Continuity
- c. Holes through Data
- d. Other Missing Text
- e. Illegible Text
- f. Duplicate Text
- g. Brief Description
- h. Sequence Listing
- i. Appendix
- j. Amendments
- k. Other

MESSAGE

MESSAGE In the renumbering of claims, claim 3 now depends on claim 4 (original claim 2) and claim 7 depends on claim 8 (original claim 12).

CLAIMS

- a. Claim(s) Missing
- b. Improper Dependence**
- c. Duplicate Numbers
- d. Incorrect Numbering
- e. Index Disagrees
- f. Punctuation
- g. Amendments
- h. Bracketing
- i. Missing Text
- j. Duplicate Text
- k. Other

Please correct dependency

THANK YOU

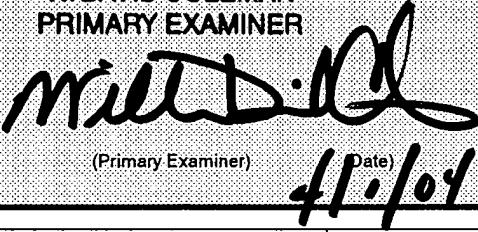
initials

RESPONSE

Corrected (i.e. renumbered) claims

initials*

Issue Classification				Application No.	Applicant(s)	
				09/665,663	UEDA, SHIGEYUKI	
				Examiner	Art Unit	
				W. David Coleman		2823

ORIGINAL				CROSS REFERENCE(S)											
CLASS		SUBCLASS		CLASS		SUBCLASS (ONE SUBCLASS PER BLOCK)									
257		777													
INTERNATIONAL CLASSIFICATION															
H	0	1	L	23/28											
H	0	1	L	23/52											
H	0	1	L	29/40											
				/											
				/											
None (Assistant Examiner) (Date)				W. DAVID COLEMAN PRIMARY EXAMINER 				Total Claims Allowed: 10							
 9/1/04 (Legal Instruments Examiner) (Date)				(Primary Examiner) 9/1/04				O.G. Print Claim(s)		O.G. Print Fig.					
1		2													

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
Final	Original	Final	Original	Final	Original	Final	Original
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2	2	32		62		92	
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4	4	34		64		94	
5	5	35		65		95	
6		36		66		96	
7	7	37		67		97	
8		38		68		98	
9		39		69		99	
8	10	40		70		100	
1	11	41		71		101	
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9	13	43		73		103	
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27		57		87		117	
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30		60		90		120	
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							210

2/1/04

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		09/665,663	UEDA, SHIGEYUKI
		Examiner	Art Unit
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cc

ISSUE CLASSIFICATION

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CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
257	777		
INTERNATIONAL CLASSIFICATION			
H 0 1 L	23/28		
H 0 1 L	23/52		
H 0 1 L	29/40		
	/		
	/		
None (Assistant Examiner) (Date)		Miller (P) W. David Coleman Primary Examiner (Primary Examiner) (Date) 12/13/03	
J. M. Short 12/15/03 (Legal Instruments Examiner) (Date)		Total Claims Allowed: 10	
		O.G. Print Claim(s)	O.G. Print Fig
		1	2

Corresponded

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant		<input type="checkbox"/> CPA		<input type="checkbox"/> T.D.		<input type="checkbox"/> R.1.47	
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28	58	88	118	148	178	208	
29	59	89	119	149	179	209	
30	60	90	120	150	180	210	

CLMPTO

12/16/03

CLAIM 1 (CANCELLED)

2. (Amended) The semiconductor chip according to claim 11, wherein said semiconductor chip is overlapped with and joined to a surface of another solid device in a state where said surface protective film is opposed to a surface of the solid device.

3. (Amended) The semiconductor chip according to claim 2, further comprising an internal connection pad which is formed by partially exposing said the internal wiring from said surface protective film in a portion of different from said external connection pad, and

an electrical contact projection formed in a raised state on the internal connection pad using a metal material having oxidation resistance in order to make electrical connection to the said solid device.

4. The semiconductor chip according to claim 2, wherein

said solid device includes another semiconductor chip.

5. (Amended) The semiconductor chip according to claim 3, wherein

said wire connecting portion is composed of the same material as that for said electrical contact projection.

CLAIM 6 (CANCELLED)

7. (Twice Amended) The semiconductor chip according to claim 12, wherein

said wire connecting portion is composed of the same material as that for said electrical contact projection.

CLAIM 8-9 (CANCELLED)

~~8~~ 10. (Amended) The semiconductor chip according to claim 12, further comprising a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connecting portion.

~~11.~~ (Amended) A semiconductor chip adapted for electrical connection to an external terminal, comprising:

a semiconductor chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the semiconductor chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad;

a surface protective film covering the internal wiring and the surface of the semiconductor chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film; and

a wire electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

1. (Amended) A semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a primary chip, wherein said primary chip comprises

a primary chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at least one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the primary chip body;

a wire connecting portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

an electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad, the electrical contact projection operative to electrically connect the primary and secondary chips together; and

a surface protective film covering the internal wiring and the surface of the primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection project from the surface protective film, wherein

the electrical contact projection is in a form of a bump and the wire connecting portion substantially has a shape of the bump.

9 - 13. (NEW) The semiconductor chip according to claim 11, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed.

10 14. (NEW) The semiconductor chip according to claim 12, wherein the wire connection portion and the electrical contact projection are made of the same material and have simultaneously been formed. -